National Semiconductor

October 1980

INS2651 Programmable Communications Interface

General Description

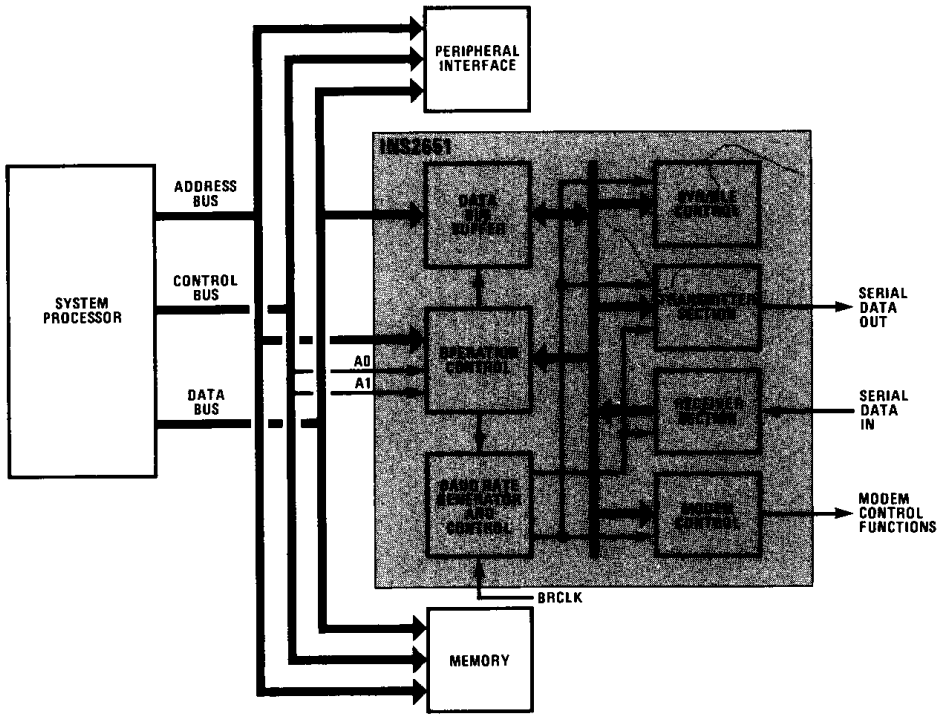
The INS2651 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as a serial data input/output interface in a bus structured system. The functional configuration of INS2651 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communications signal presently in use.

The INS2651 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS2651 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS2651 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS2651, as well as error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Selectable 1 or 2 SYNC Characters
  - Transparent or Non-Transparent Mode
  - Automatic SYNC or DLE-SYNC Insertion
  - SYNC or DLE Stripping
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x, or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 0.8 M Baud (Synchronous)
  - DC to 0.8 M Baud (1x, Asynchronous)
  - DC to 50 k Baud (16x, Asynchronous)
  - DC to 12.5 k Baud (64x, Asynchronous)
- Internal or External Baud Rate Clock
  - 16 Internal Rates (50 to 19,200 Baud)
- Double Buffering of Data
- TTL Compatible
- No System Clock Required
- Direct Plug-In Replacement for Signetics 2651

INS2651 General System Configuration



TL/G/PG-FL20M100 Printed in U.S.A.

Absolute Maximum Ratings

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Voltages with Respect to Ground	−0.5 V to +6.0 V

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.*

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%, GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage		0.25	0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	2.8		V	I_{OH} = −100 μA
I_{IL}	Input Load Current			10	μA	V_{IN} = 0 V to 5.5 V
I_{LD}	Data Bus Leakage Current			10	μA	V_{OUT} = 4.0 V
I_{LO}	Open Drain Leakage Current			10	μA	V_{OUT} = 4.0 V
I_{CC}	Power Supply Current		65	150	mA	

Capacitance

T_A = +25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			20	pF	f_c = 1 MHz
C_{OUT}	Output Capacitance			20	pF	Unmeasured pins
$C_{I/O}$	I/O Capacitance			20	pF	to ground

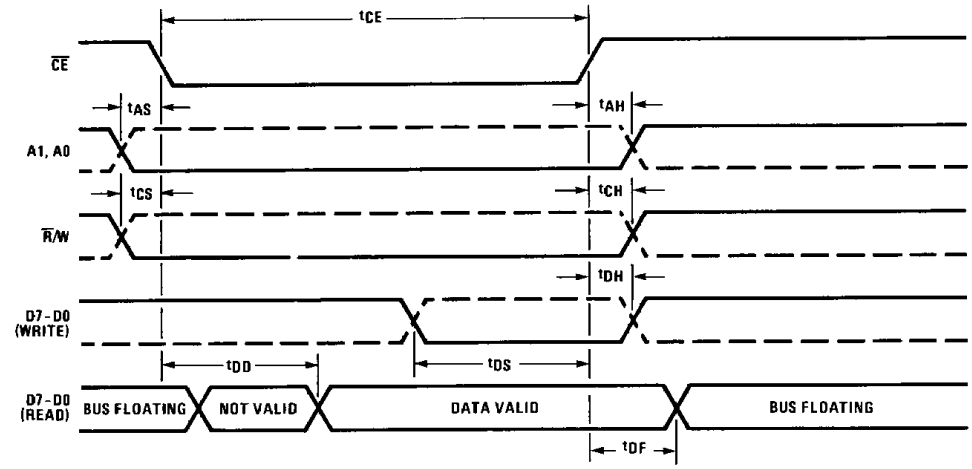
AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%, GND = 0 V

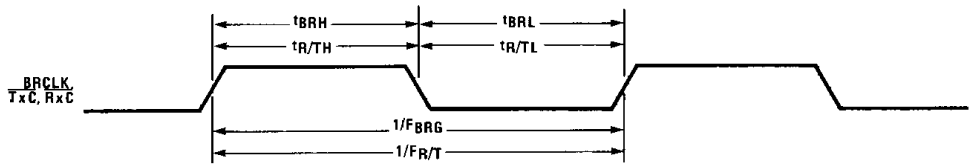
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
BUS PARAMETERS						
t_{CE}	Chip Enable Pulse Width	300			ns	
t_{AS}	Address Setup Time	20			ns	
t_{AH}	Address Hold Time	20			ns	
t_{CS}	$\overline{R}$/W Control Setup Time	20			ns	
t_{CH}	$\overline{R}$/W Control Hold Time	20			ns	
t_{DS}	Data Setup Time for Write	225			ns	
t_{DH}	Data Hold Time for Write	50			ns	
t_{DD}	Data Delay Time for Read			250	ns	C_L = 100pF
t_{DF}	Data Bus Floating Time for Read			150	ns	C_L = 100pF
OTHER TIMINGS						
t_{RES}	RESET Pulse Width	1000			ns	
f_{BRG}	Baud Rate Generator Input Clock Frequency	1.0	5.0688	5.073	MHz	
t_{BRH}	Baud Rate Clock High State	70			ns	
t_{BRL}	Baud Rate Clock Low State	70			ns	
$f_{R/T}$	$\overline{TxC}$ or $\overline{RxC}$ Input Clock Frequency	DC		0.769	MHz	
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ Clock High State	650			ns	
$t_{R/TL}$	$\overline{TxC}$ or $\overline{RxC}$ Clock Low State	650			ns	
t_{TxD}	TxD Delay from Falling Edge of $\overline{TxC}$			650	ns	C_L = 100pF
t_{TCS}	Skew Between TxD Changing and Falling Edge of $\overline{TxC}$ Output		0	0	ns	C_L = 100pF
t_{RxS}	Rx Data Setup Time	300			ns	
t_{RxH}	Rx Data Hold Time	300			ns	

Timing Waveforms

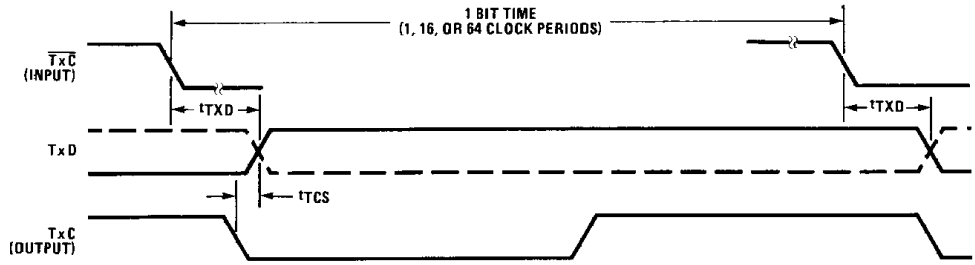
RESET TIMING



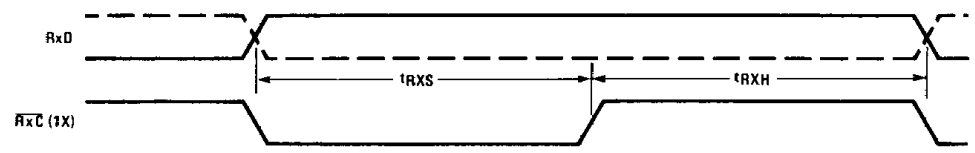
READ AND WRITE TIMING



CLOCK TIMING

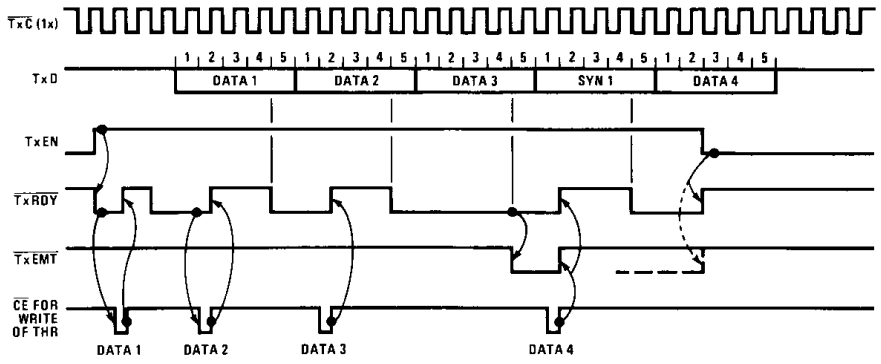


TRANSMIT TIMING

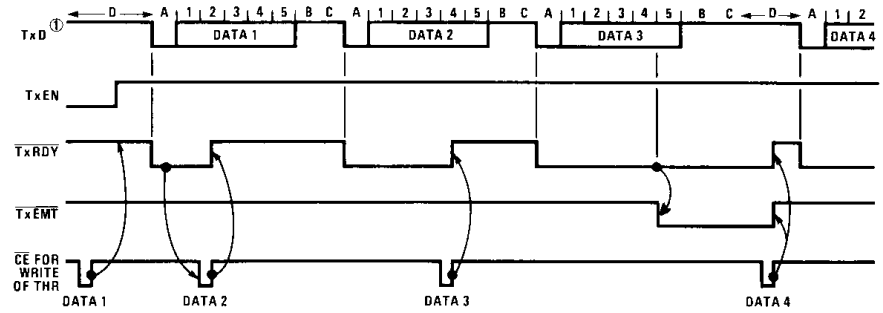


RECEIVE TIMING

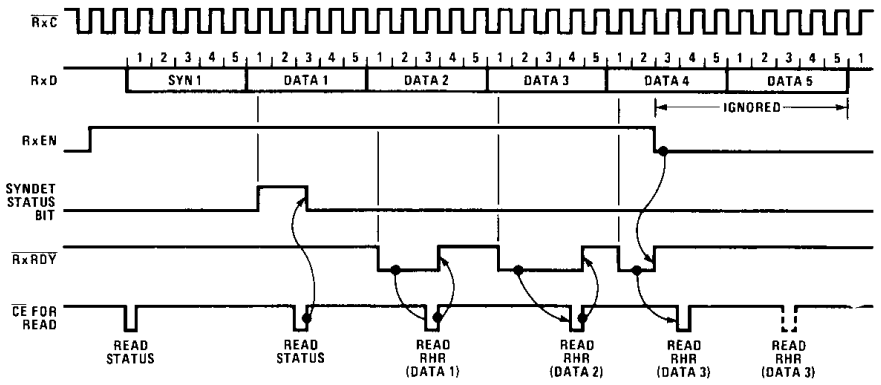
Timing Waveforms (cont'd.)



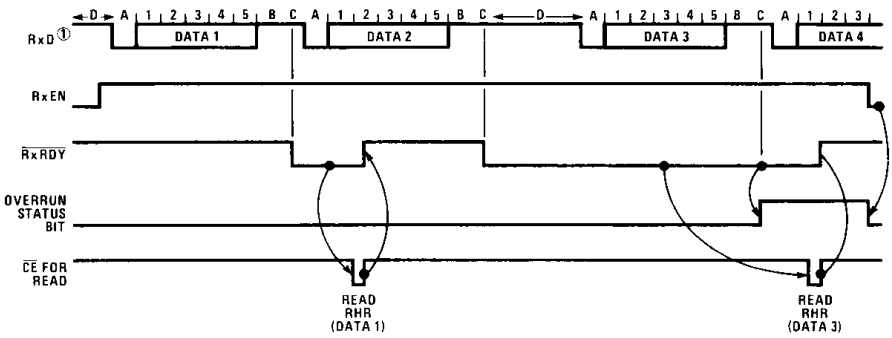
SYNCHRONOUS MODE



ASYNCHRONOUS MODE



SYNCHRONOUS MODE

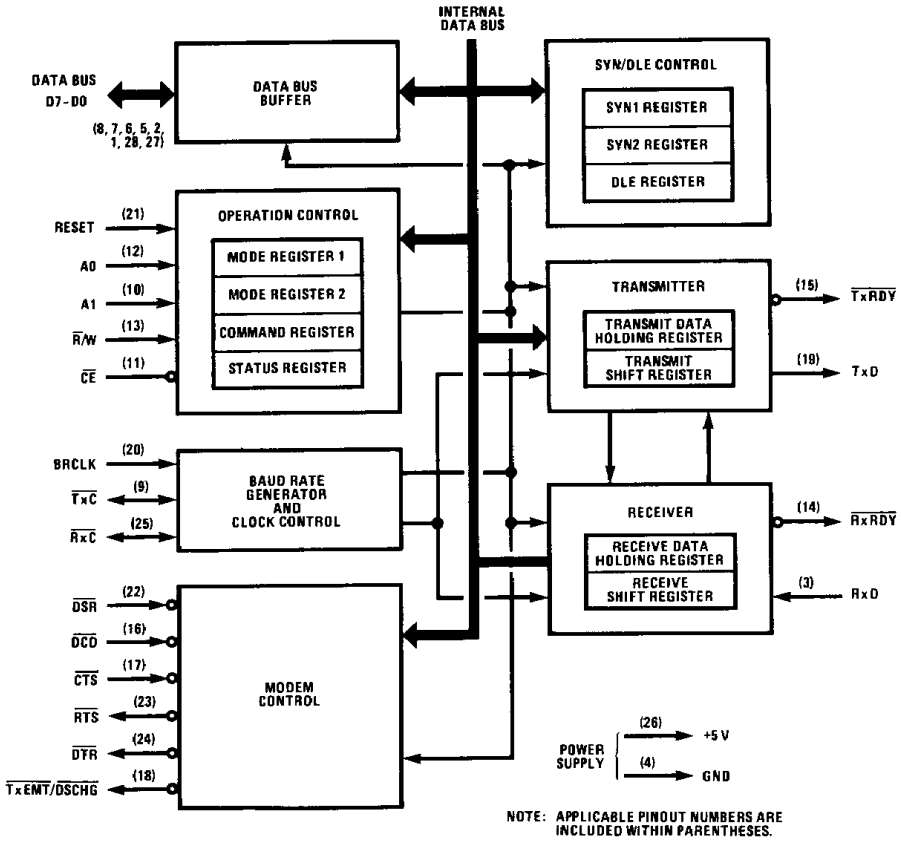


ASYNCHRONOUS MODE

TxRDY, TxEMT TIMING (SHOWN FOR 5-BIT CHARACTERS, NO PARITY, 2-STOP BITS (IN SYNCHRONOUS MODE).
RxRDY TIMING (SHOWN FOR 5-BIT CHARACTERS, NO PARITY, 2-STOP BITS (IN ASYNCHRONOUS).

NOTE 1: A – START BIT, B – STOP BIT 1, C – STOP BIT 2,
D – TxD MARKING CONDITION.

INS2651 Block Diagram



INS2651 Functional Pin Definitions

The following describes the function of all the INS2651 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Reset (RESET), Pin 21: When high, performs a master reset on the INS2651. This signal asynchronously terminates any device activity and clears the Mode, Command, and Status Regsiters. The device assumes the idle state and remains in this mode until initialized with the appropriate control words.

Address Lines (A1-A0), Pins 10, 12: Address lines used to select internal Mode and Command registers.

Read/Write ($\overline{R}$/W), Pin 13: Controls the direction of data bus transfers. A high input allows data from the CPU to be loaded into the addressed register. A low input causes the contents of the addressed register to be present on the data bus.

Chip Enable ($\overline{CE}$), Pin 11: When low, indicates that control and data lines to the device are valid and that the specified operation should be performed. When high, places the device in the TRI-STATE® condition.

Baud Rate Generator Clock (BRCLK), Pin 20: 5.0688 MHz clock input to the internal Baud Rate Generator. Not required if external receiver and transmitter ($\overline{TxC}$ and $\overline{RxC}$) clocks are used.

Receiver Data (RxD), Pin 3: Serial data input to the receiver.

Data Set Ready ($\overline{DSR}$), Pin 22: General-purpose input which, when low, indicates either the Data Set Ready or Ring condition. Its complement is stored as Status Register bit 7. A change in state of this input causes a low output on $\overline{TXEMT/DSCHG}$.

Data Carrier Detect ($\overline{DCD}$), Pin 16: When low, enables the receiver to operate. The complement of this input is stored as Status Register bit 6, and an input change in state causes a low output on $\overline{TXEMT/DSCHG}$.

Clear to Send ($\overline{CTS}$), Pin 17: When low, enables the transmitter to operate. When high, holds the $\overline{TxD}$ output in MARK condition.

V_{CC}, Pin 26: +5-volt supply.

Ground, Pin 4: 0-volt reference.

OUTPUT SIGNALS

Transmitter Ready ($\overline{TxRDY}$), Pin 15: A low on this output, which is open-drain, indicates that Transmit Holding Register (THR) is ready to accept a data character from the CPU. This output, which is the complement of Status Register bit 0, goes high when the data character is loaded and is valid only when the transmitter is enabled. The $\overline{TxRDY}$ output can be used as an interrupt to the system.

Receiver Ready ($\overline{RxRDY}$), Pin 14: A low on this output, which is open-drain, indicates that the Receive Holding Register (RHR) has a character ready for input to the CPU. This output, which is the complement of Status Register bit 1, goes high either when the Receiver Holding Register is read by the CPU or when the receiver is disabled. The $\overline{RxRDY}$ output can be used as an interrupt to the system.

Transmitter Empty or Data Set Change ($\overline{TxEMT/DSCHG}$), Pin 18: A low on this output, which is open-drain, indicates that either the transmitter has completed serialization of the last character loaded by the CPU or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. If the TxEMT condition does not exist, this output goes high when the Status Register is read by the CPU. Otherwise, the Transmit Holding Register must be loaded by the CPU for this line to go high. The $\overline{TxEMT}$/$\overline{DSCHG}$ output can be used as an interrupt to the system. This output is the complement of Status Register bit SR2.

Transmitter Data ($\overline{TxD}$), Pin 19: Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) when the transmitter is disabled.

Data Terminal Ready ($\overline{DTR}$), Pin 24: General-purpose output normally used to indicate Data Terminal Ready. The $\overline{DTR}$ output is the complement of Command Register bit 1.

Request to Send ($\overline{RTS}$), Pin 23: General-purpose output normally used to indicate Request to Send. The $\overline{RTS}$ output is the complement of Command Register bit 5.

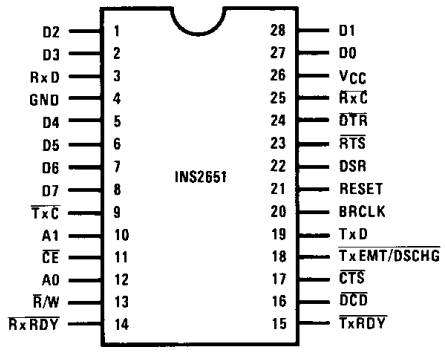
INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus, Pins 28, 27, 8, 7, 6, 5, 2, 1: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS2651 and the CPU. Data, control words, and status information are transferred via the Data Bus.

Receiver Clock ($\overline{RxC}$), Pin 25: If external receiver clock is programmed, this input controls the rate at which a data character is received. The frequency of the $\overline{RxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Transmitter Clock ($\overline{TxC}$), Pin 9: If external transmitter clock is programmed, this input controls the rate at which a data character is transmitted. The frequency of the $\overline{TxC}$ input is a multiple (1x, 16x, or 64x) of the Baud Rate. Transmitter Data is clocked out of the INS2651 on the falling edge of the $\overline{TxC}$ input. If internal transmitter clock is programmed, this pin becomes an output at 1x the programmed Baud Rate.

Pin Configuration



INS2651 Programming

The system software determines the operative conditions (mode selection, clock selection, data format, and so forth) of the INS2651 via internal Mode Registers 1 and 2, and the Command Register. Prior to initiating data communications, the INS2651 operational mode must be programmed by performing write operations to these 8-bit registers via the Data Bus. The device can be reprogrammed at any time during program execution. However, the receiver and transmitter should be disabled if the change has an effect on the reception or transmission of a character.

The internal registers of the INS2651 are accessed by applying signals to the $\overline{CE}$, $\overline{R}/W$, A1, and A0 inputs as specified in table 1.

Table 1. Guess My Name

$\overline{CE}$	A1	A0	R/W	Function
1	X	X	X	TRI-STATE Data Bus
0	0	0	0	Read Receive Holding Register
0	0	0	1	Write Transmit Holding Register
0	0	1	0	Read Status Register
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers 1 and 2
0	1	0	1	Write Mode Registers 1 and 2
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

In the case of multiple registers (SYN1/SYN2/DLE Registers and Mode Registers 1 and 2), successive read or write operations will access the next higher register. For example, if A1 equals 0, A2 equals 1, and $\overline{R}/W$ equals 1, the first write operation loads SYN1 Register. The next write operation loads SYN2 Register, and the third loads the DLE Register. Read and write operations are performed on the Mode Registers in a similar manner. If more than the required number of accessses is made, the internal register pointer returns to the first register. The pointers are reset to the first registers either by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

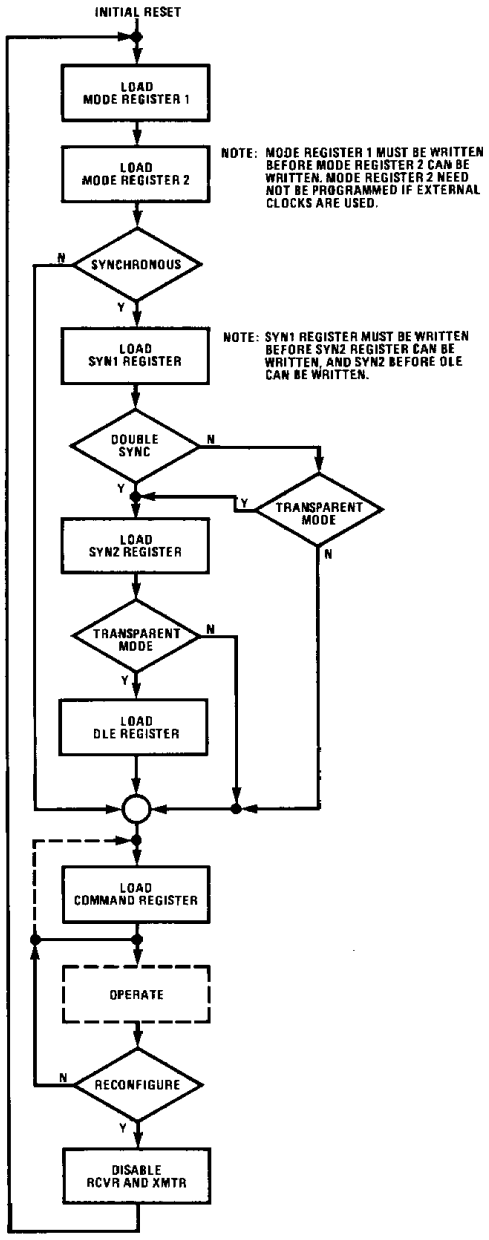


Figure 1. Initialization Flowchart

MODE REGISTER 1 FORMAT

BIT NUMBERS

MR1-7	MR1-6	MR1-5	MR1-4	MR1-3	MR1-2	MR1-1	MR1-0

SYNC:
NO. OF SYN CHARACTERS
0 = DOUBLE SYN
1 = SINGLE SYN

SYNC:
TRANSPARENCY CONTROL
0 = NORMAL
1 = TRANSPARENT

PARITY TYPE
0 = ODD
1 = EVEN

PARITY CONTROL
0 = DISABLED
1 = ENABLED

CHARACTER LENGTH
00 = 5 BITS
01 = 6 BITS
10 = 7 BITS
11 = 8 BITS

MODE AND BAUD RATE FACTOR[1]
00 = SYNCHRONOUS 1x RATE
01 = ASYNCHRONOUS 1x RATE
10 = ASYNCHRONOUS 16x RATE
11 = ASYNCHRONOUS 64x RATE

ASYNC:
STOP BIT LENGTH
00 = INVALID
01 = 1 STOP BIT
10 = 1½ STOP BITS
11 = 2 STOP BITS

MODE REGISTER 2 FORMAT

BIT NUMBERS

MR2-7	MR1-6	MR2-5	MR2-4	MR2-3	MR2-2	MR2-1	MR2-0

NOT USED

TRANSMITTER CLOCK
0 = EXTERNAL
1 = INTERNAL

RECEIVER CLOCK
0 = EXTERNAL
1 = INTERNAL

BAUD RATE SELECTION

0000 = 50 BAUD	0110 = 600 BAUD	1100 = 4800 BAUD
0001 = 75 BAUD	0111 = 1200 BAUD	1101 = 7200 BAUD
0010 = 110 BAUD	1000 = 1800 BAUD	1110 = 9600 BAUD
0011 = 134.5 BAUD	1001 = 2000 BAUD	1111 = 19200 BAUD
0100 = 150 BAUD	1010 = 2400 BAUD	
0101 = 300 BAUD	1011 = 3600 BAUD	

COMMAND REGISTER FORMAT

BIT NUMBERS

CR-7	CR-6	CR-5	CR-4	CR-3	CR-2	CR-1	CR-0

OPERATING MODE
00 = NORMAL OPERATION
01 = ASYNC: AUTOMATIC ECHO MODE
SYNC: SYN AND/OR DLE STRIPPING MODE
10 = LOCAL LOOP BACK
11 = REMOTE LOOP BACK

REQUEST TO SEND
0 = FORCES $\overline{RTS}$ OUTPUT HIGH
1 = FORCES $\overline{RTS}$ OUTPUT LOW

RESET ERROR
0 = NORMAL
1 = RESET ERROR FLAG IN STATUS REGISTER (FE, OE, PE/DLE DETECT)

ASYNC:
FORCE BREAK
0 = NORMAL
1 = FORCE BREAK
SYNC:
SEND DLE
0 = NORMAL
1 = SEND DLE

RECEIVE CONTROL (RxEN)
0 = DISABLE
1 = ENABLE

DATA TERMINAL READY
0 = FORCES $\overline{DTR}$ OUTPUT HIGH
1 = FORCES $\overline{DTR}$ OUTPUT LOW

TRANSMIT CONTROL
0 = DISABLE
1 = ENABLE

STATUS REGISTER FORMAT

BIT NUMBERS

SR-7	SR-6	SR-5	SR-4	SR-3	SR-2	SR-1	SR-0

DATA SET READY
0 = $\overline{DSR}$ INPUT IS HIGH
1 = $\overline{DSR}$ INPUT IS LOW

DATA CARRIER DETECT
0 = DCD INPUT IS HIGH
1 = DCD INPUT IS LOW

FE/SYN DETECT
ASYN:
0 = NORMAL
1 = FRAMING ERROR
SYNC:
0 = NORMAL
1 = SYN CHARACTER DETECTED

OVERRUN
0 = NORMAL
1 = OVERRUN ERROR

PE/DLE DETECT
ASYNC:
0 = NORMAL
1 = PARITY ERROR
SYNC:
0 = NORMAL
1 = PARITY ERROR OR DLE CHARACTER RECEIVED

TxEMT/DSCHG
0 = NORMAL
1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY

RxRDY
0 = RECEIVE HOLDING REGISTER EMPTY
1 = RECEIVE HOLDING REGISTER HAS DATA

TxRDY
0 = TRANSMIT HOLDING REGISTER BUSY
1 = TRANSMIT HOLDING REGISTER EMPTY

NOTE 1: BAUD RATE FACTOR IN ASYNCHRONOUS MODE APPLIES ONLY IF EXTERNAL CLOCK IS SELECTED. FACTOR IS 16x IF INTERNAL CLOCK IS SELECTED.

Table 2. Baud Rate Generator Characteristics (Crystal Frequency = 5.0688 MHz)

Baud Rate	Theoretical Frequency 16x Clock (kHz)	Actual Frequency 16x Clock (kHz)	Percent Error	Duty Cycle (%)	Divisor
50	0.8	0.8	–	50/50	6336
75	1.2	1.2	–	50/50	4224
110	1.76	1.76	–	50/50	2880
134.5	2.152	2.1523	0.016	50/50	2355
150	2.4	2.4	–	50/50	2112
300	4.8	4.8	–	50/50	1056
600	9.6	9.6	–	50/50	528
1200	19.2	19.2	–	50/50	264
1800	28.8	28.8	–	50/50	176
2000	32.0	32.081	0.253	50/50	158
2400	38.4	38.4	–	50/50	132
3600	57.6	57.6	–	50/50	88
4800	76.8	76.8	–	50/50	66
7200	115.2	115.2	–	50/50	44
9600	153.6	153.6	–	48/52	33
19200	307.2	316.8	3.125	50/50	16

Note: 16x clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1x and duty cycle is 50%/50% for any baud rate.

INS2651 Operation

GENERAL

The transmitter section of the INS2651 performs parallel-to-serial conversion of data supplied to it from the system data bus.

The receiver section of the INS2651 performs serial-to-parallel conversion of data received from the MODEM or input/output device. Both the transmitter and receiver are double buffered, allowing a full character time in which to service Transmit Ready ($\overline{TxRDY}$) and Receive Ready ($\overline{RxRDY}$) interrupts.

The character size (5, 6, 7, or 8 bits) is program selectable. Parity check/generation and the baud rate may also be defined by the program. Note that the character size is exclusive of the start/stop and parity bits.

SYNCHRONOUS MODE

The transmitter starts transmitting a continuous bit stream once the transmitter is enabled and the Clear to Send ($\overline{CTS}$) input is low. If the system is late in supplying a character to the transmitter, then the transmitter will send the SYN character (or SYN1, two characters if in double SYNC mode) as an idle fill in the Non-Transparent mode, or the DLE-SYN1 character pair as an idle fill in the Transparent mode. If this condition occurs, the $\overline{TxEMT/DSCHG}$ output goes low.

The receiver enters a character synchronization mode as soon as the receiver is enabled and the Data Carrier Detect ($\overline{DCD}$) input goes low. Either one or two consecutive SYN characters must be recognized by the receiver. The number of SYN characters is program selectable, and data is sent to the processor only after synchronization. The SYN character(s) in the Transparent mode (or DLE-SYN1 characters in the Non-Transparent mode) are stripped off the data stream after synchronization. This feature is program selectable.

An overrun error will occur if the processor is late in servicing the received character. When this condition occurs, the character in the receiver buffer is written over by the character causing the overrun, and the overrun status bit is set.

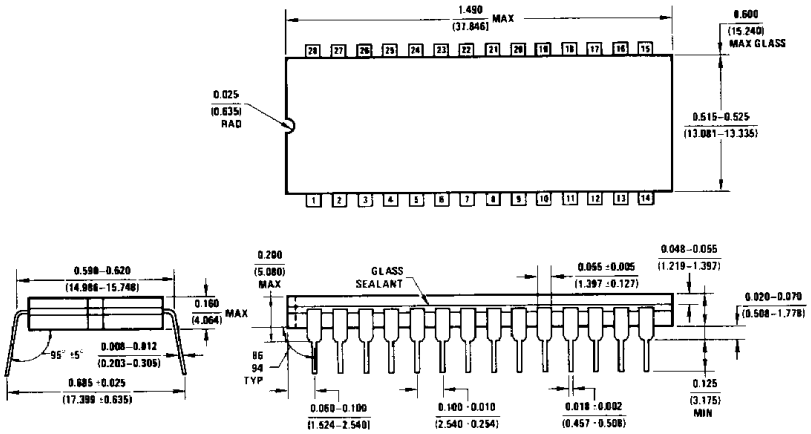
ASYNCHRONOUS MODE

Once transmission is initiated, the transmitter supplies the start bit, odd, even, or no parity bit, and the proper number of stop bits as specified by the program. If the next character is presented to the transmitter, it is sent immediately after transmission of the stop bit of the present character. Otherwise the Mark (logic high) condition is sent. The transmitter can be programmed to send a Space (logic low) condition instead of the Mark condition.

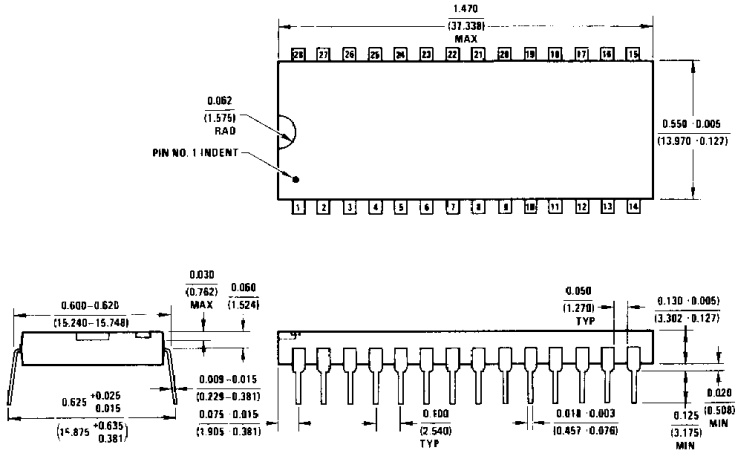
Once the receiver is enabled, reception of a character is initiated by recognition of the start bit. The Start/Stop and Parity bits are stripped off while assembling the serial input into a parallel character. If a break condition is detected then the receiver sends a character of all zero bits and a Framing Error status bit to the processor.

Succeeding all-zero or break characters are not assembled and presented to the system. The Receive Data (RxD) input must return to a marking condition before character assembly is resumed. The overrun condition is checked in the same manner as in the Synchronous mode.

Physical Dimensions



28-Lead Ceramic Dual-In-Line Package [Cer Dip (J)]
Order Number INS2651J



28-Lead Plastic Dual-In-Line Package (N)
Order Number INS2651N

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